CLAIMS

What is claimed is:

1. A method for protecting a semiconductor process wafer surface from contacting thermally degraded photoresist comprising the steps of:

providing a semiconductor process wafer having a process surface;

forming a protective layer over selected areas of the process surface said protective layer including a resinous organic material having a glass transition temperature (Tg) that is about greater than a thermal treatment temperature;

forming a photoresist layer over at least a portion of the protective layer to include a photolithographic patterning process; and

subjecting the semiconductor process wafer to the thermal treatment temperature.

2. The method of claim 1, wherein the glass transition temperature (Tg) is greater than about 300 degrees Centigrade.

3. The method of claim 1, wherein the protective layer comprises Benzocyclobutene.

4. The method of claim 3, wherein the glass transition temperature (Tg) is greater than about 350 degrees Centigrade.

5. The method of claim 1, wherein prior to the step including the thermal treatment temperature a portion of the protective layer is removed to reveal an under bump metal layer for forming a solder column thereover.

6. The method of claim 5, wherein the solder column is formed within a photoresist stencil included in the photoresist layer.

7. The method of claim 6, wherein the thermal treatment temperature is according to a reflow process carried out on the solder column.

8. The method of claim 7, wherein the solder column includes a lead content of greater than about 90 weight percent.

9. The method of claim 1, wherein the protective layer includes at least one under bump metal layer (UBM) for forming a solder ball thereover.

10. The method of claim 1, wherein the protective layer is removable by at least one of reactive ion etching and wet chemical stripping.

11. An improved method for forming a solder ball in a semiconductor chip bonding process comprising the steps of:

providing a semiconductor wafer process surface including at least one under bump metal (UBM) layer overlying a chip bonding pad said at least one under bump metal (UBM) layer including a contact layer for forming a solder bump thereover;

forming a protective layer overlying the semiconductor wafer process surface including the contact layer said protective layer including a resinous organic material having a glass transition temperature (Tg) that is greater than a thermal treatment temperature;

forming a photoresist layer over the protective layer to include a photolithographic patterning process for forming a stencil pattern including an opening for containing a solder column overlying the contact layer;

removing a portion of the protective layer to reveal the contact layer for forming the solder column thereover;

forming the solder column over the contact layer; and

subjecting the solder column to the thermal treatment temperature to induce solder reflow.

12. The method of claim 11, wherein the glass transition temperature (Tg) is greater than about 300 degrees Centigrade.

13. The method of claim 11, wherein the protective layer comprises Benzocyclobutene.

14. The method of claim 13, wherein the glass transition temperature (Tg) is greater than about 350 degrees Centigrade.

15. The method of claim 11, wherein the solder column includes a lead content of greater than about 90 weight percent.

16. The method of claim 11, wherein the at least one under bump metal layer (UBM) includes at least one of titanium, copper, and nickel.

17. The method of claim 11, wherein the protective layer is removable by at least one of reactive ion etching and wet chemical stripping.

18. The method of claim 11, further comprising the step of removing the photoresist layer and underlying protective layer by a wet chemical stripping process.

19. The method of claim 11, wherein the step of providing a semiconductor wafer process surface including at least one under bump metal (UBM) layer further includes depositing a UBM masking photoresist layer over the at least one UBM layer; and reactive

ion etching the lowermost UBM layer to reveal a passivation layer surrounding a chip bonding pad area;

20. The method of claim 18, further comprising the step of performing a second solder reflow process to form a solder ball.